

Towards Instruction Set Consolidation

Fred Weber — CTO, Computation Products Group

Future innovation should come in micro-architecture enhancements and compatible extensions to dominant instruction sets, rather than the creation of new instruction sets.

1

Is the trend clear?

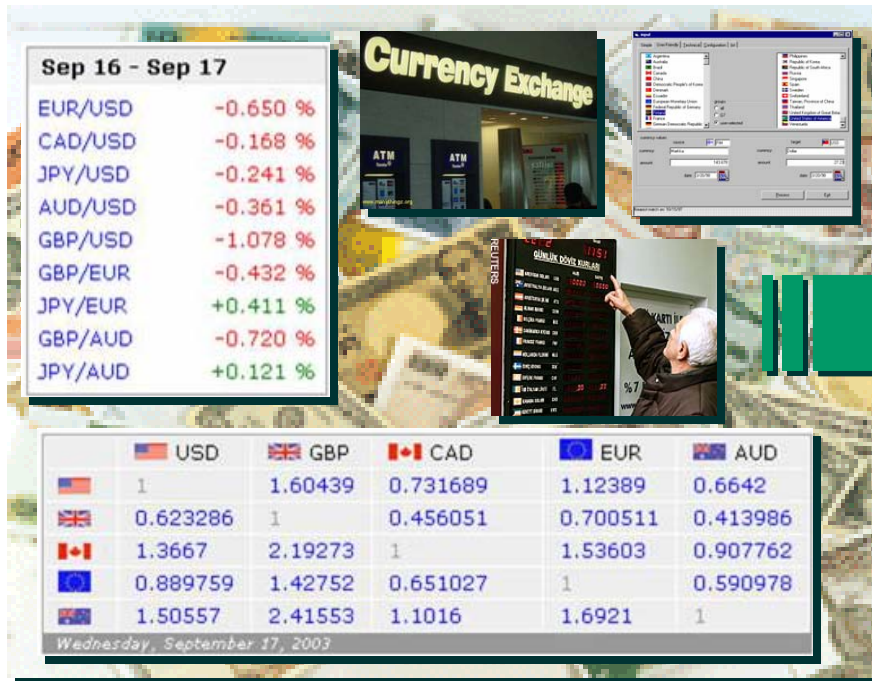
With ever growing software complexity and installed base the value of remaining compatible with and extending existing, dominant instruction sets heavily outweighs any disadvantages.

2

Is the time now?

Technology has passed the point where instruction set costs are at all relevant.

The economic benefits of moving away from multiple currencies is enormous.



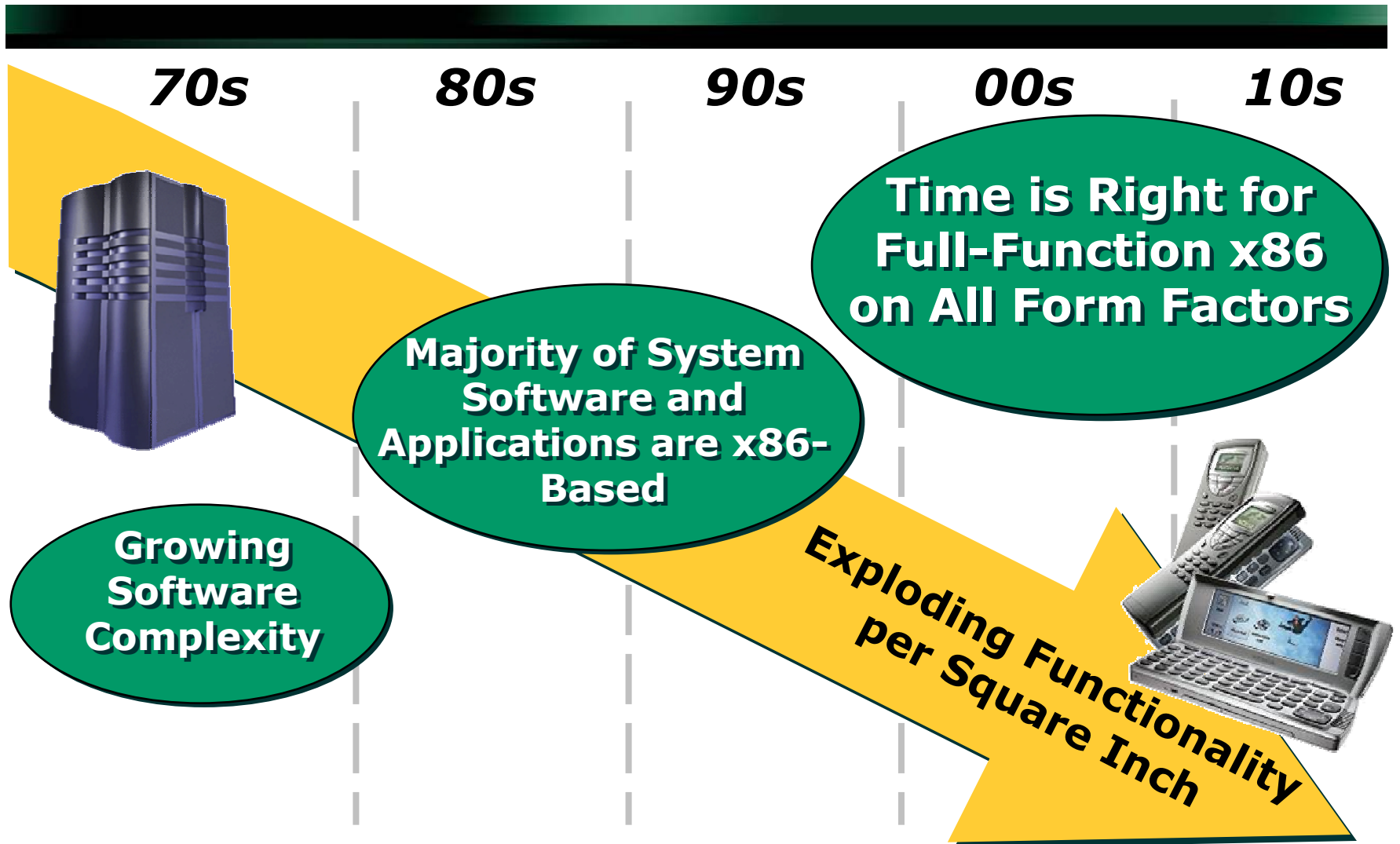
\$36 billion per year in avoided transaction costs, or \$90 per EU resident

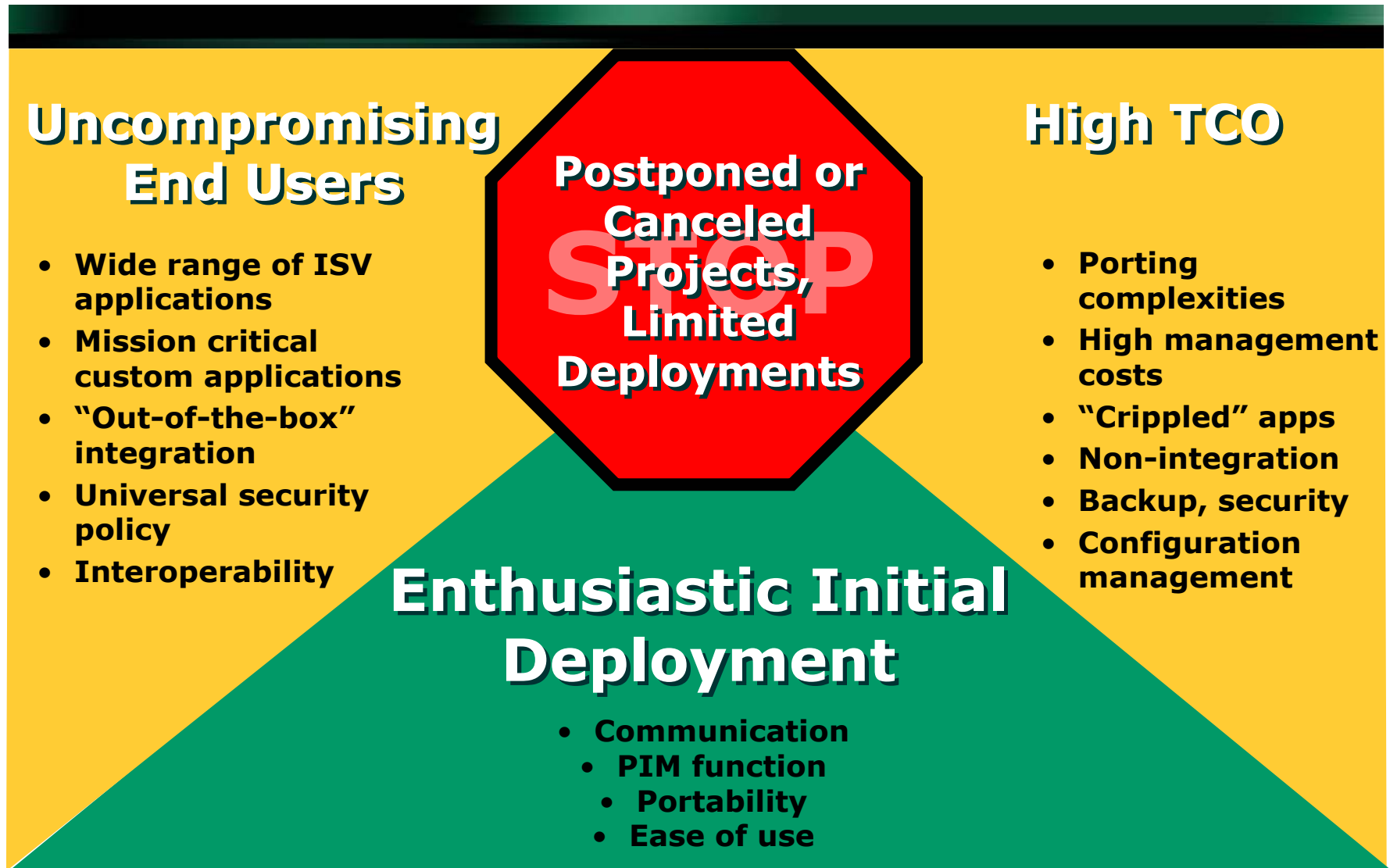
What were the catalysts that prompted standardization?

- ✓ **Growing markets**
- ✓ **More sophisticated consumers**
- ✓ **Desire for increased stability**

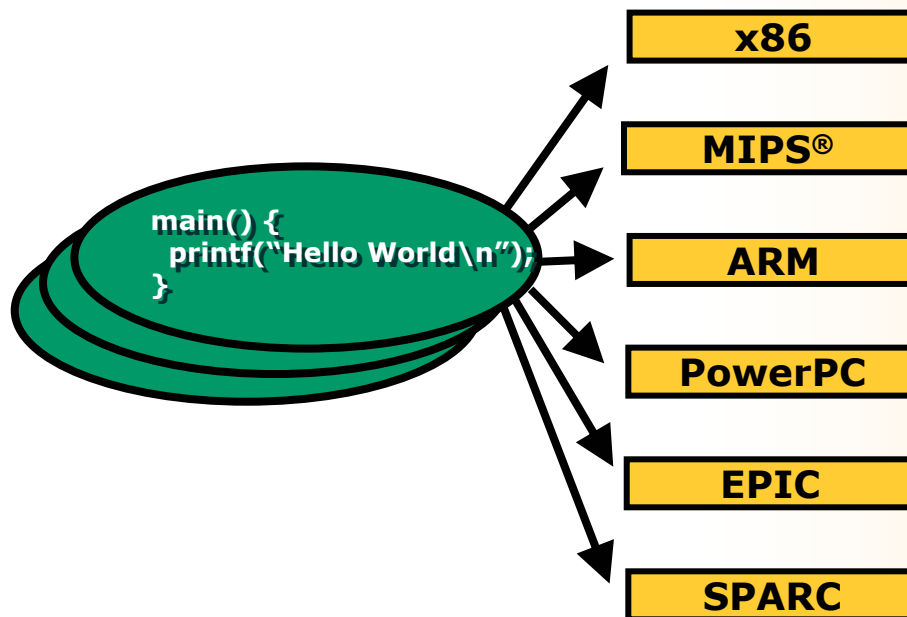


Architectural Evolution Macro-Level



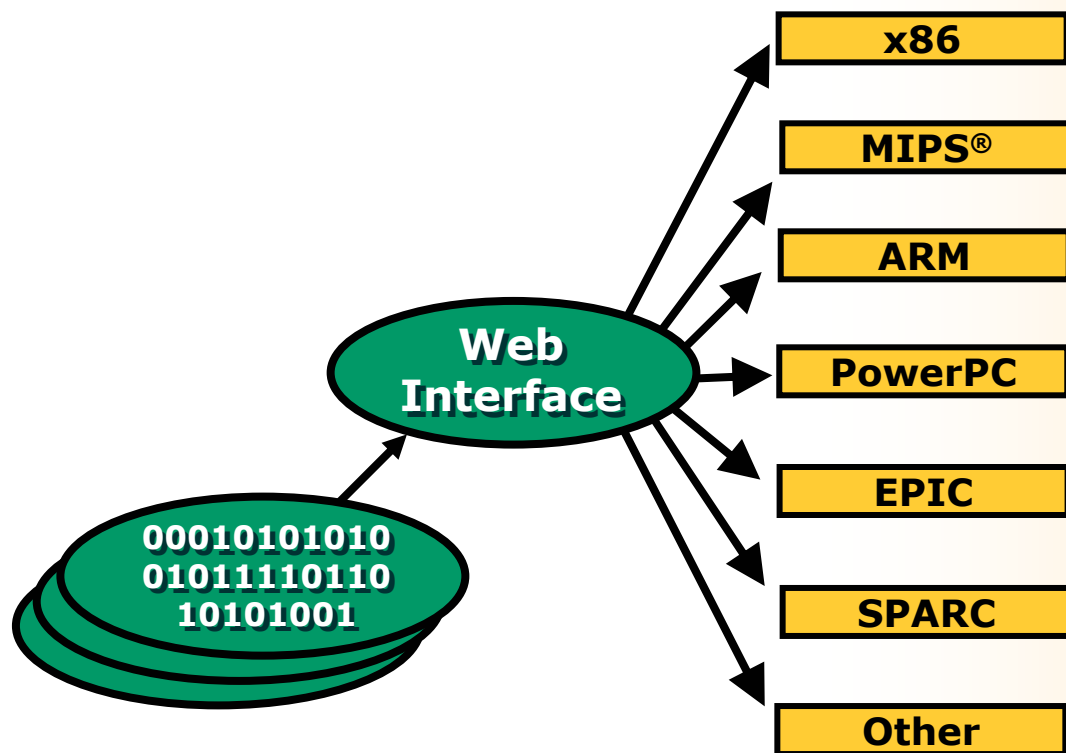


Port thousands of applications, operating systems, drivers, codecs, tool chains and virtual machines.



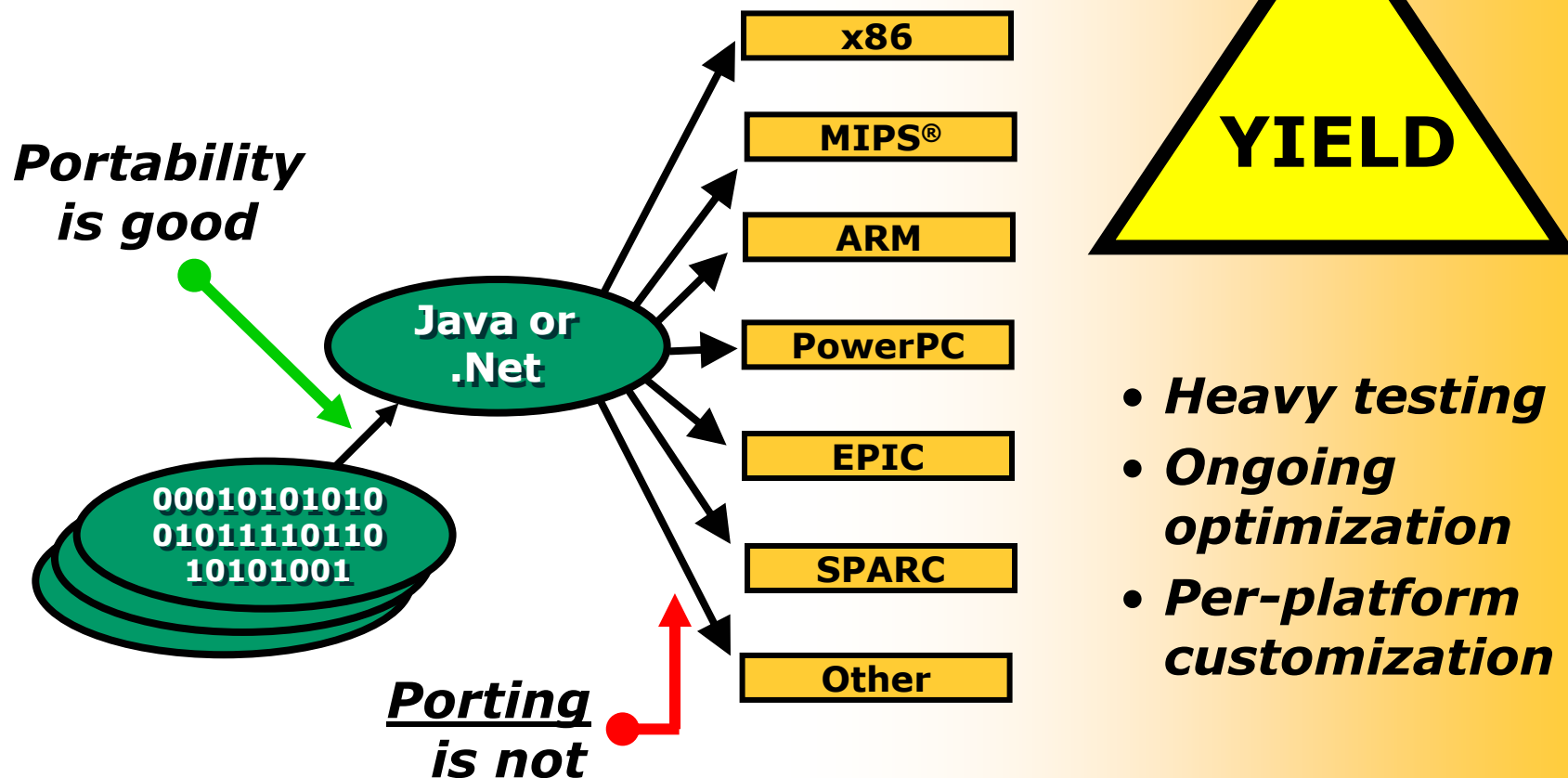
- ***Resource intensive***
- ***Slow***
- ***Costly to maintain***

Develop a web-based interface for each application.



- *Assumes always-connected client server*
- *Limited functionality*
- *Difficult security*

Write once (or port once) and run anywhere.



Executing and/or translating to multiple languages and platforms is a necessary cost — not something to be desired.



Architectural Evolution Macro-Level



Common Instruction Set Architecture

No need to port

**No need for multiple
validations**

**Built in OS
integration**

Robust security

**Investment
protection**

— The Future? —

Happening Now

Today

Networking

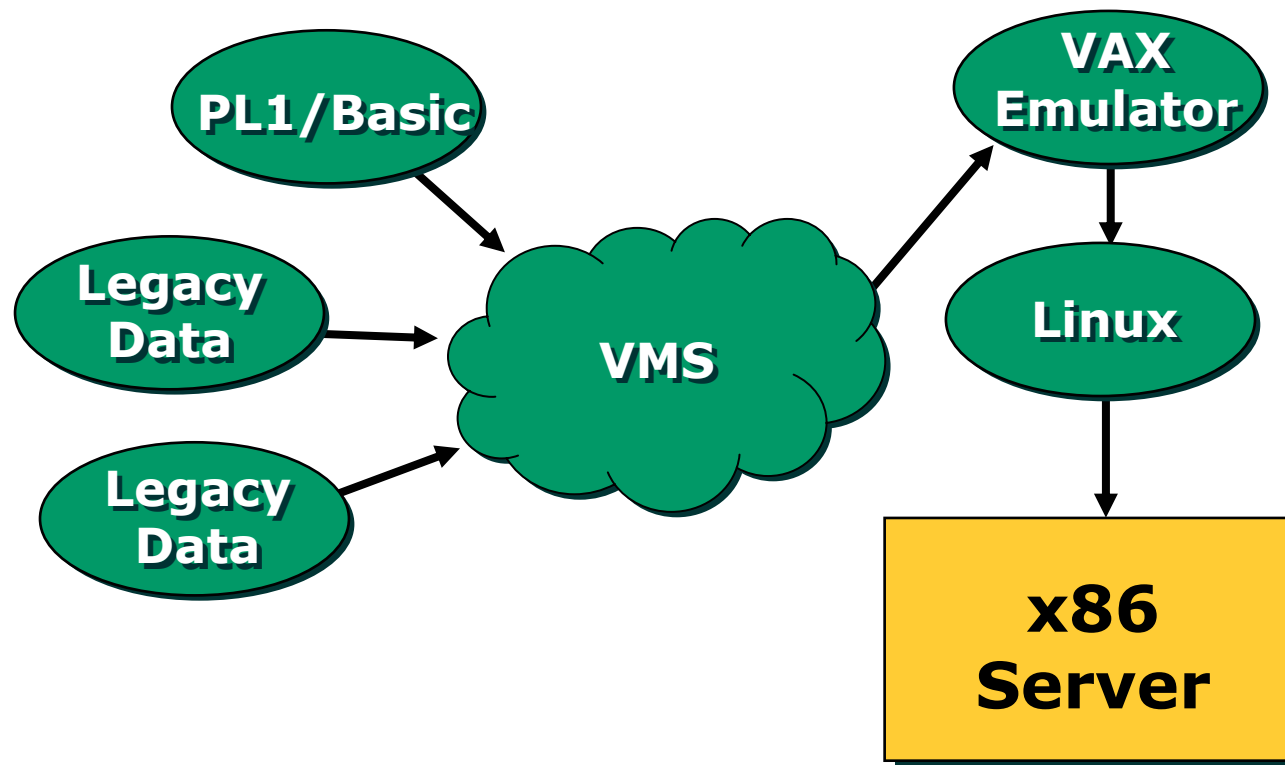
Storage

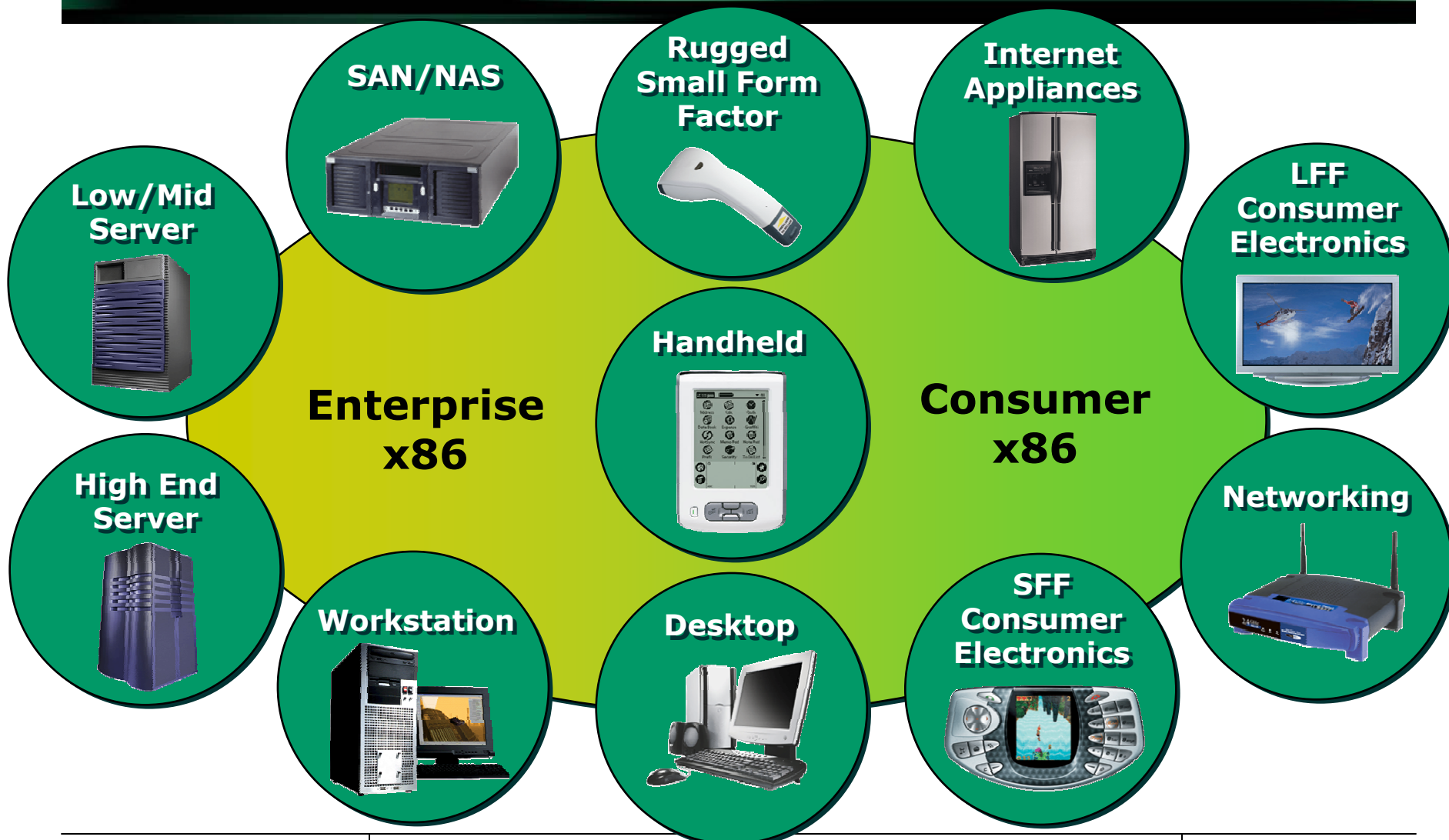
**Server
Desktop
Laptop**

Handheld

Ubiquitous

Essential legacy data and code lives forever.

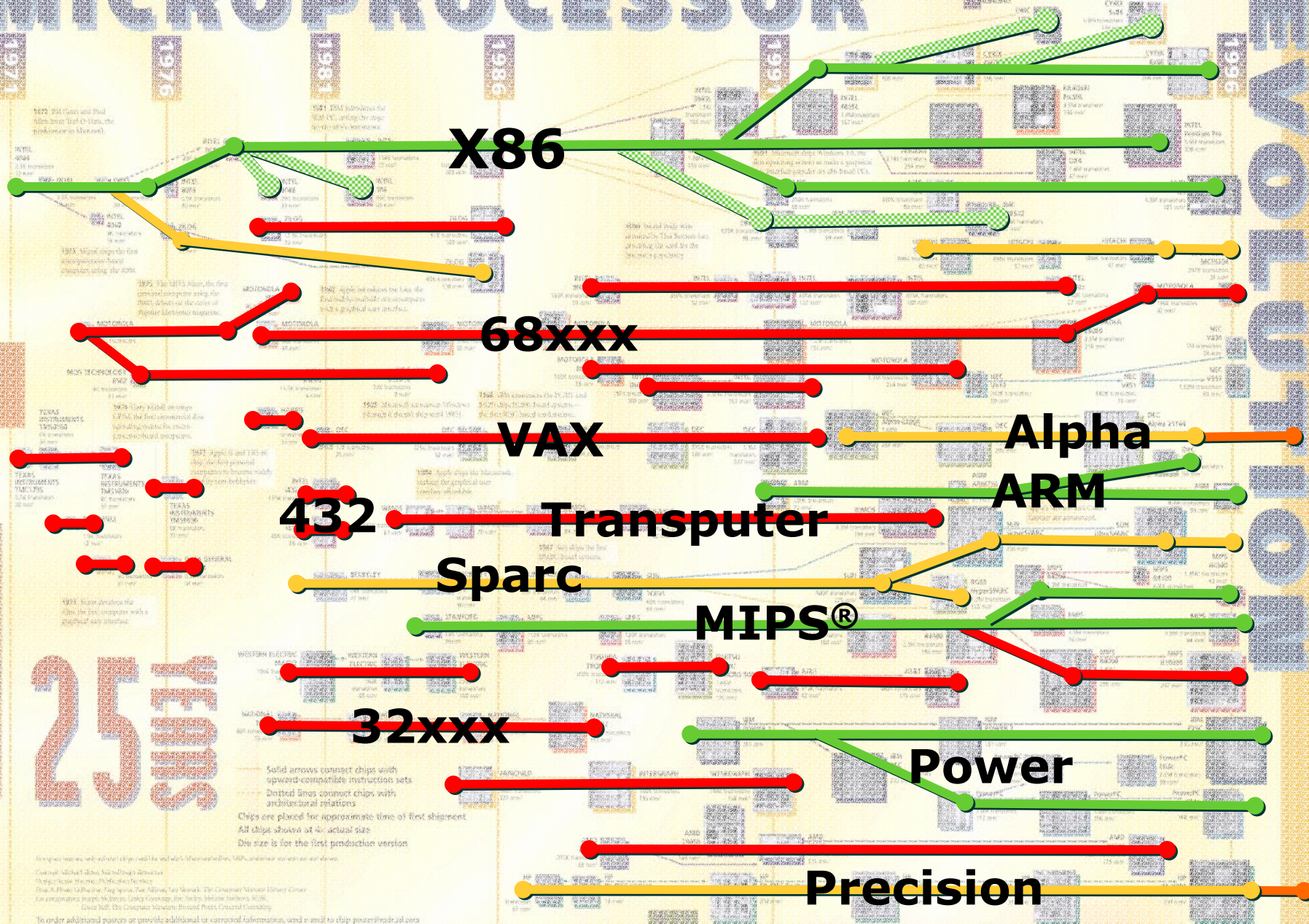




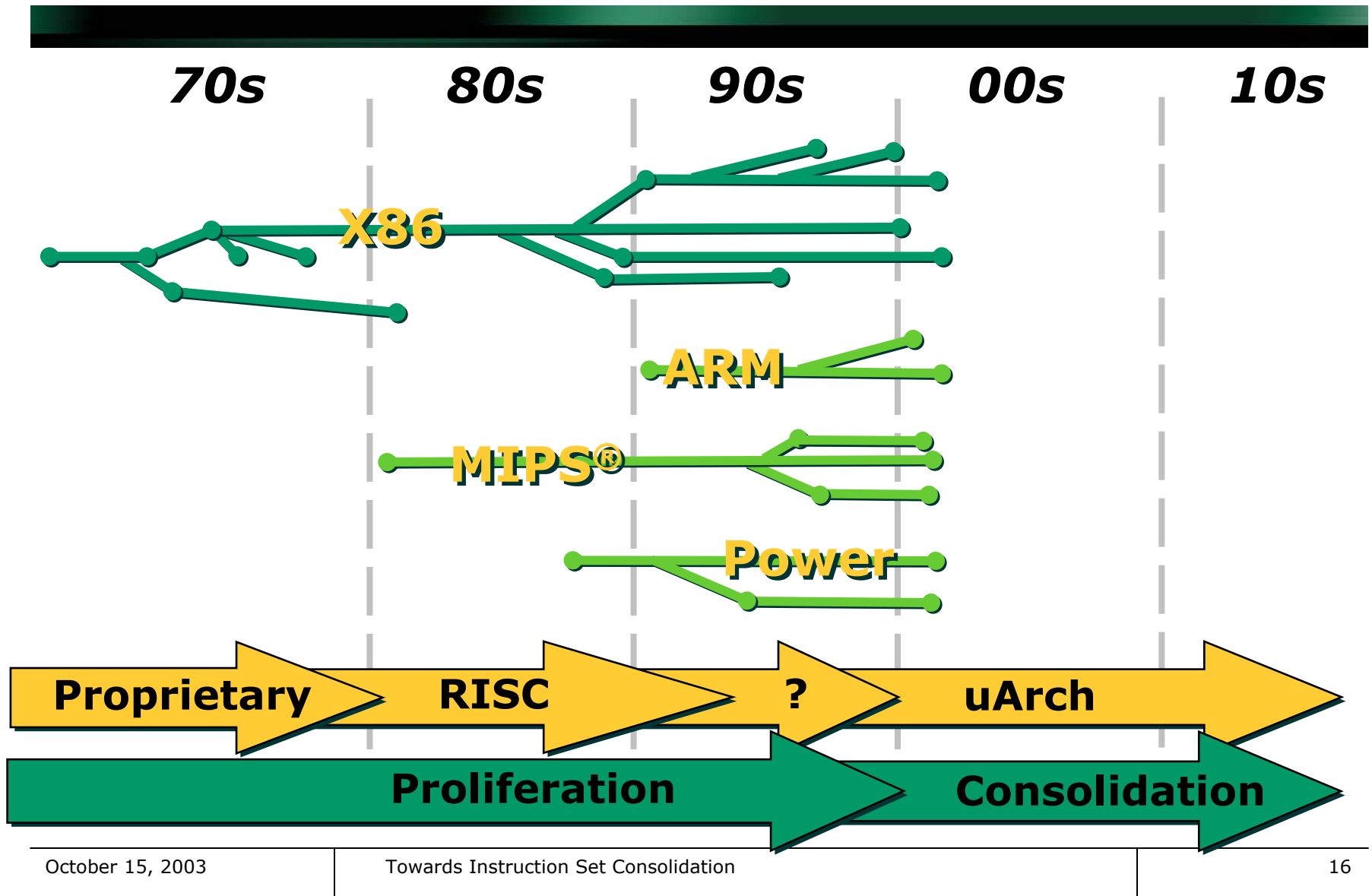
Vaughan Pratt

Chairman and CTO, Tiqit Computers

THE 40 F G L O



Architectural Evolution

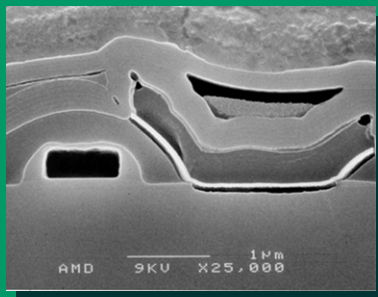


Why is It Possible Now?

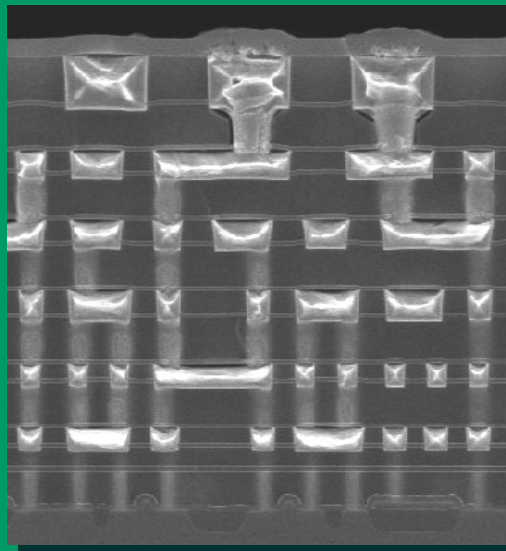


- Moore's Law
 - Core processors can now be so small that any overhead of x86 is easily affordable (a few mm², a few % of total die, trivial power increment)
- Sufficiency of performance
 - Means CPU designs can range from small simple designs to huge server designs
- Added functionality makes processor core small part of chip
 - Large L1 and L2 cache
 - SOC functions (memory control, graphics, etc.)
- Pads fundamentally force minimum die size much larger than core
- Learning
 - Lots of design tricks have accumulated

**AMD Am386®
Processor**
2 Alum. layer
1.0μ design rules

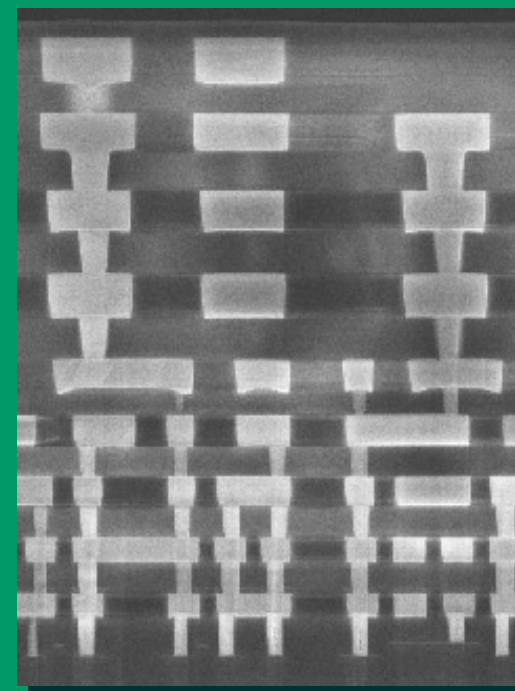


**AMD Athlon™
Processor**
6 Copper layer
180 nm design rules

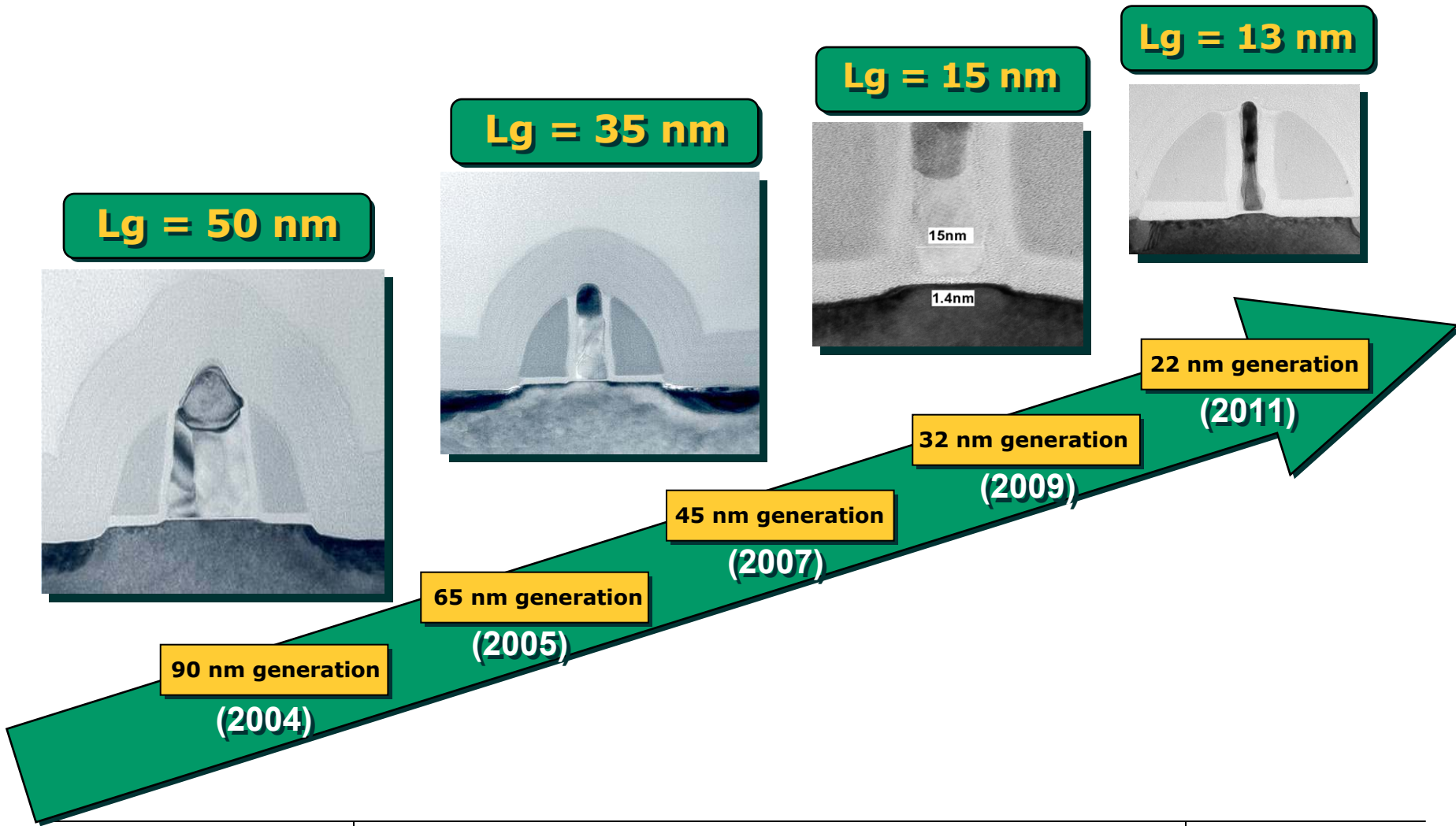


**AMD Athlon™ 64
Processor**

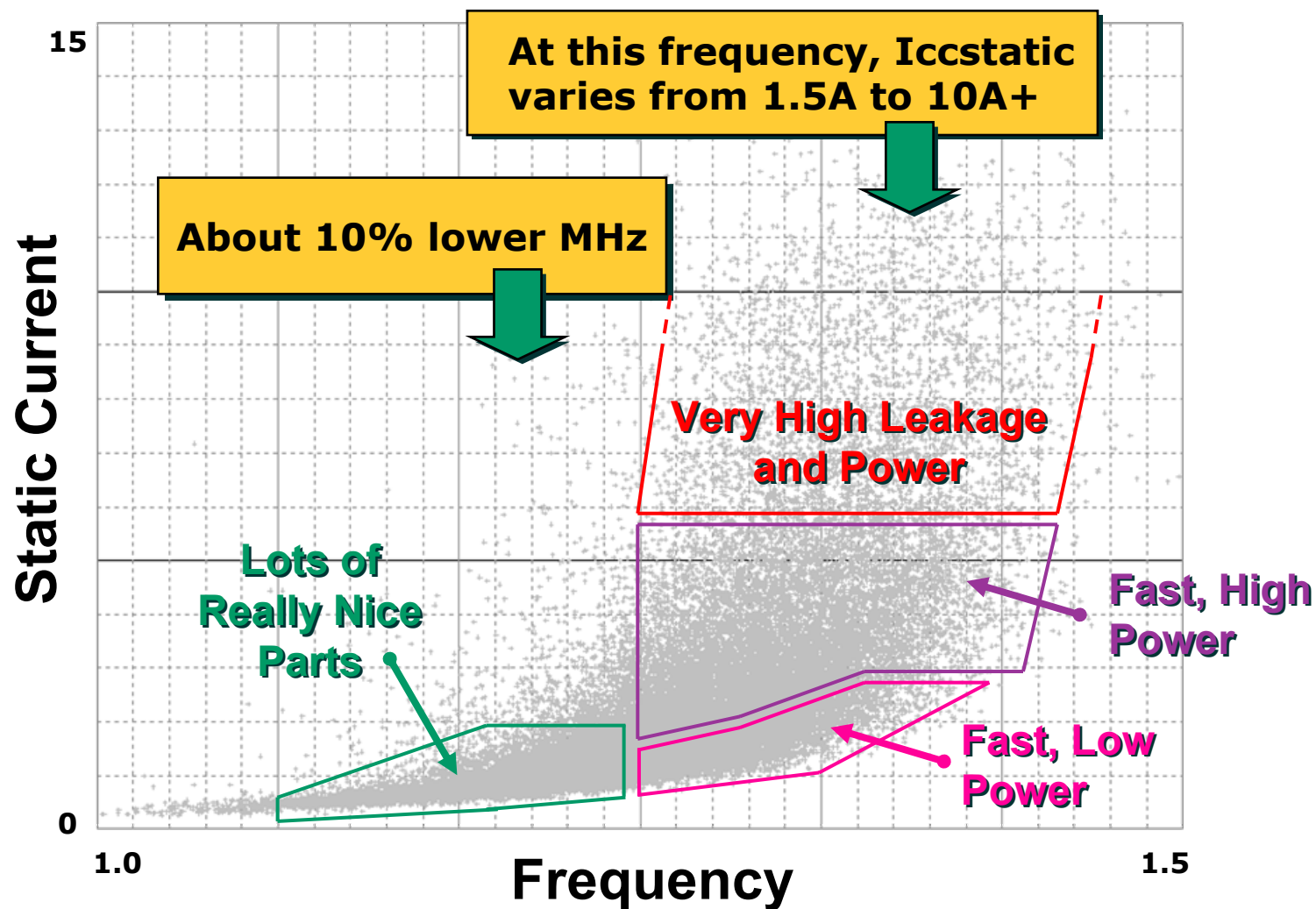
9 Copper layer
130 nm design rules



Planned Transistor Evolution



Huge Variation – Without Even Trying!



Primary Drivers of Performance, Power and Cost



Performance

Memory Latency – We Have Hit the Memory Wall

- At 1GHz and 1 IPC a 1% effective miss rate cuts performance by approx. 50%, 4% cuts it by approx. 80%
- Required IPC, application footprint and DRAM speed dictate cache size

Peak Instruction Rate

- Determined by IPC and MHz

Power

Dynamic

- Voltage
- Switching capacitance
 - Number of parallel units
 - Number of flops (pipeline depth)
 - Clock skew goal
 - Long buses
 - Clock gating

Static

- Process: Gate leakage, Dcap leakage and Ioff
- Voltage and temperature
- Total transistor width
 - Leaky transistor width if substantial use of low leakage transistors

Cost

Package, Assembly and Test

- 25-50% of total cost

Cache and IO Often Dominate Die Size

- IO often in the range of 15-20% of die area
- Cache can be as much as 50% of the die area or more

Dynamic Range of Design Choices



Lever	Range	Factor
Pipeline Depth	5-25 stages	5x
Cache	16K-2M bytes	125x
ILP	1-10 units	10x
Voltage	0.7-1.4 volts	2x
IO Pins	100-500	5x
Frequency	300-3000 MHz	10x
Leakage (Idoff)	1-1000 nA/um	1000x
Die Size	30-300 mm ²	10x
Dynamic Power	0.2-100 W	500x

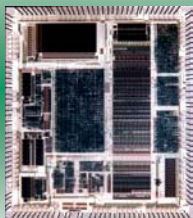
***All can be varied
independent of
instruction set.***

Three Orders of Magnitude Transistor Count



16 —————> 32 —————> 64 Bits
Integer —————> FPU, SIMD Vector
1/3 Issue —————> 9 Issue
Trivial Cache —————> 1MB Cache
CPU —————> SOC

**AMD
Am386[®]
Processor**



**0.8 μ
200K
transistors
48mm²**

**AMD
Am486[®]
Processor**



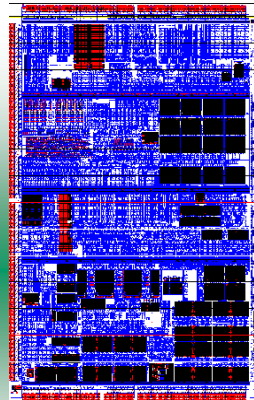
**0.35 μ
1.2M
transistors
35mm²**

**AMD K6[®]-III
Processor**



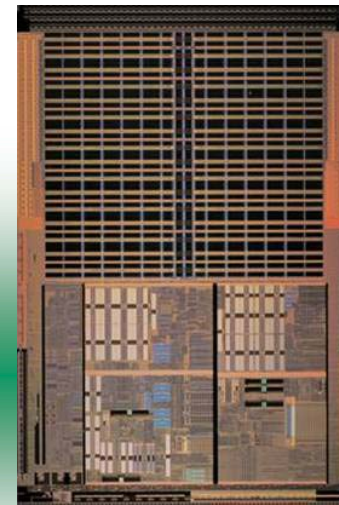
**0.25 μ
9M
transistors
78mm²**

**AMD
Athlon[™]
Processor**



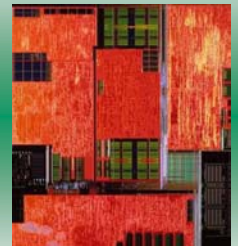
**0.18 μ
37M
transistors
120mm²**

**AMD
Opteron[™]
Processor**



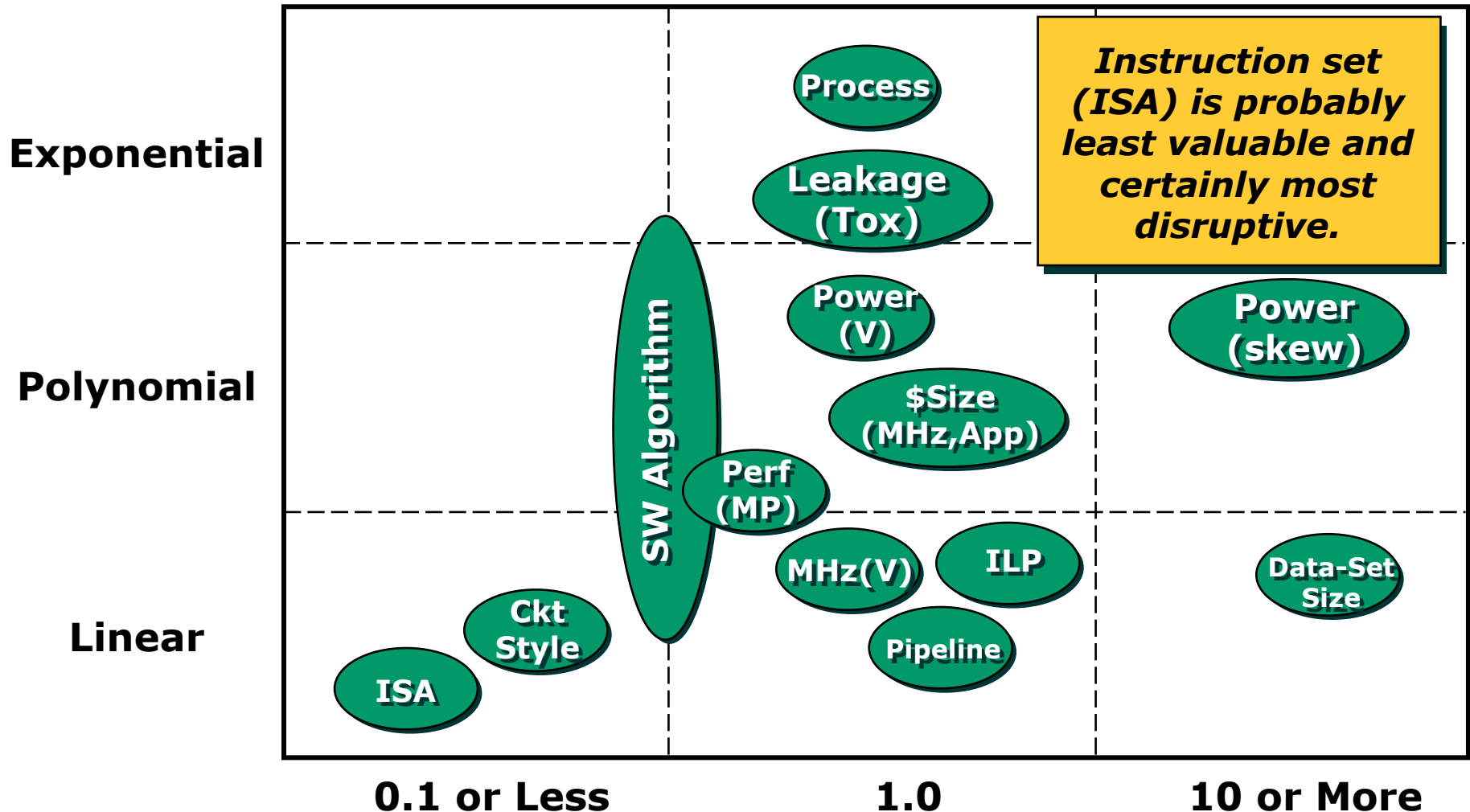
**0.13 μ
100M
transistors
193mm²**

**AMD
Geode[™]
Processor**

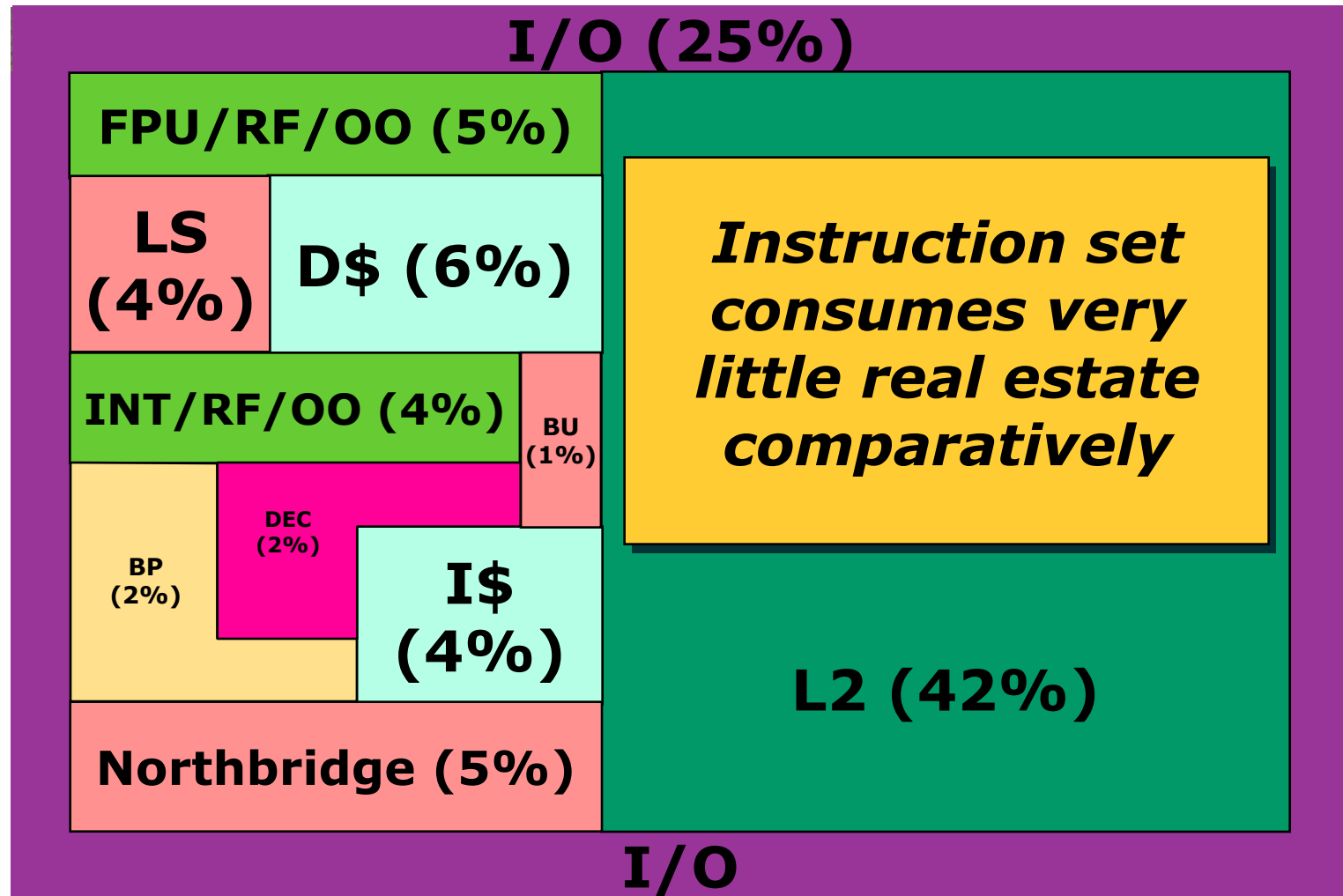


**0.15 μ
9.5M
transistors
58.3mm²**

Levers Affecting Performance, Power and Cost



Absolute Costs Demonstrate the Time is Now



Absolute Costs Demonstrate the Time is Now



1M Transistors	1mm ²
64KB Cache	1mm ²
1mm²	10-20 cents
Package pin	0.5-2 cents
200 pin package	\$1-\$4
500 pin package	\$5-\$10
512KB Cache	\$1-\$2
Small CPU Core	5mm ² , \$0.5-1
Substantial CPU Core	40mm ² , \$4-\$8

***... and so,
instruction set
adds very little
cost.***

- Threaded architectures
- 10GHz operation
- Chip level multiprocessing
- Huge scale MP machines
- Much higher performance superscalar, out of order CPU core
- Media/vector processing extensions
- Security and virtualization
- Huge caches
- Static and dynamic Power management
- Branch and memory hints
- GHz performance IO

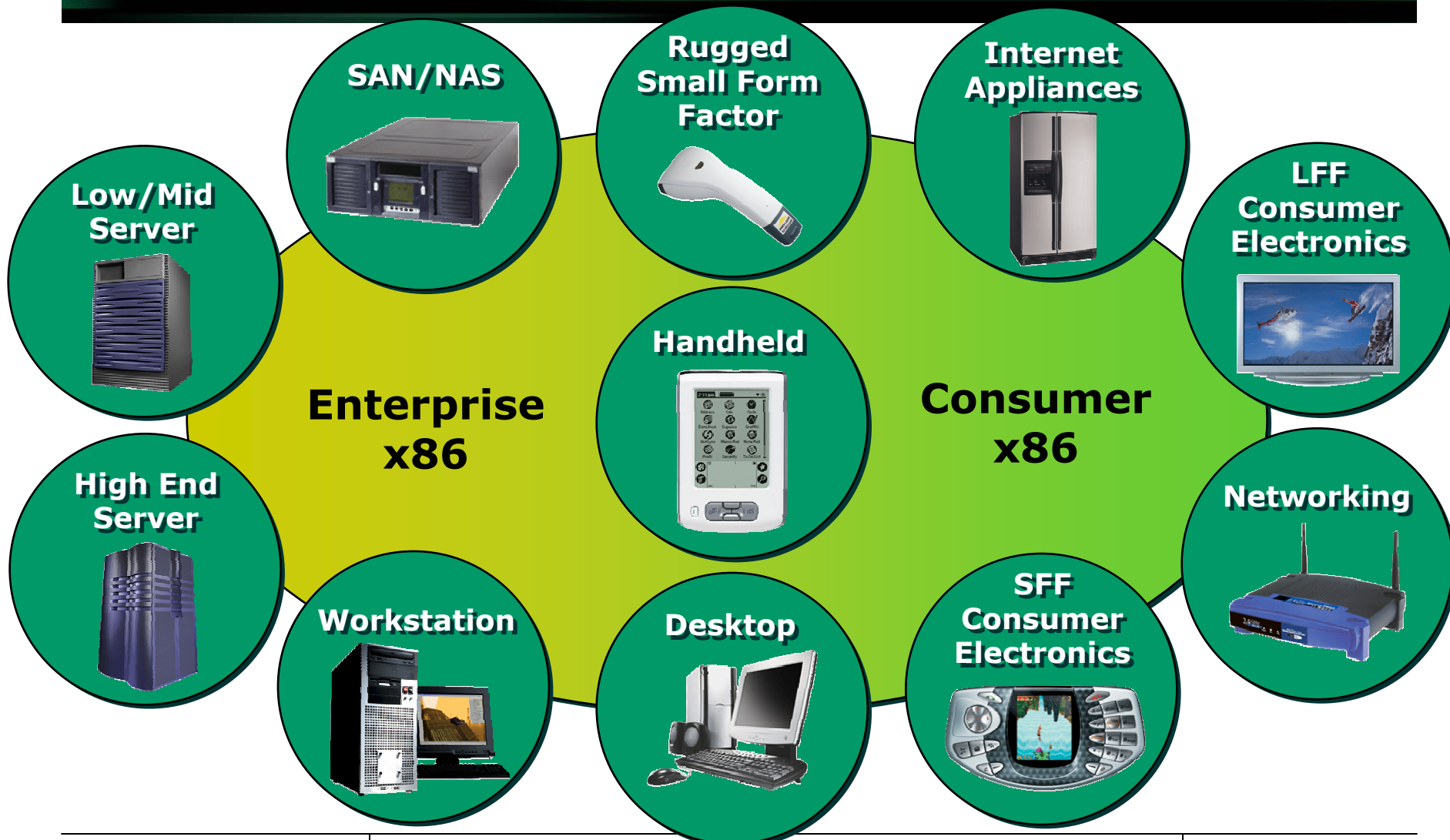
***All are
essentially
instruction
set agnostic.***



The trend is clear. The time is now.

**Instruction Set Architecture
Consolidation**

Micro-Architecture Proliferation



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